Remarks

The above Amendments and these Remarks are in reply to the Office action mailed July 26, 2005. Claims 1-32 are presented herewith for consideration.

Currently, claims 1-32 are pending. Applicants have amended claims 1, 12. Applicants respectfully request reconsideration of claims 1-25.

I. Summary of the Examiner's Objections and Rejections

Claim 12 was objected to because of the following informalities: on line 2, the recitation, "the decision transistor" appears to be --the decision switch--.

Claims 1, 2, 4, 6, 12-15, 19, 20, 23, and 24 were rejected under 35 U.S.C. 102(b) as being anticipated by *Iroaga et al.* (US 2002/0191315 A1).

Claims 3, 5, 7-11, 16-18, 21, 22, and 25 were objected to as being dependent upon a rejected base claim.

II. Summary of the Amendments

Claims 1 and 12 have been amended herein.

III. Remarks

It is respectfully submitted that the informality with respect to claim 12 has been amended and the Examiner's objection to the claim is now moot.

It is further respectfully submitted that claims 1-25, as amended, are not anticipated under 35 U.S.C. § 102(b) by US Patent 6,700,719 to *Iroaga et al.*

Independent claim 1 of the present application now defines "a decision switch ... enabling a current path from the first input to the second output only when a voltage present at said first output reaches a threshold."

Support for this amendment can be found in the specification at page 10, lines 12-17.

> The gate of transistor mp11, generally referred to herein as the "decision" transistor, will also be at a voltage of LVCasBias – V(mn9). Since mp11 is only "on" when its gate voltage is less than LVCasBias less the threshold voltages of mn8 and mp11, mp11 stays off until the voltage at out- approaches zero. As OUT- approaches zero, the source of mn9 drops and mp11 turns on. (Specification, page 10, lines 12-17).

The Examiner alleges that transistor 204 is a decision switch. However, *Iroaga et al.* does not disclose a decision switch.

As claimed, a decision switch coupled to a current sink enables a current path from the first input to the second output only when a voltage present at said first output reaches a threshold.

Transistor 204 does not "enable ... only when a voltage present at said first output reaches a threshold." Transistor 204 does not respond to changes in voltage at the first output (taps A or B). Transistor 204 does not enable any current path when the voltage at the first output changes. Thus, transistor 204 does not enable a current path from the first input to the second output only when a voltage present at said first output reaches a threshold.

Iroaga et al. discloses the function of transistor 204 at column 4 lines 3 – 40, which states in part:

> the voltage drop across the resistor 209, resistor 210, and resistor 211 is equal to the resistance of resistor 213 times the current I_2. This is true because of the connection of transistor 203 and transistor 204 ... Thus, the current I_3 is equal to the current I_4 ... thus, since the same current flows through transistor 203 and transistor 204, the emitter resistance of the respective transistors 203 and 204 are the same resulting in a low common mode rejection. (*Iroaga et al.*, col. 4 lines 8-12).

With reference to figure 2, *Iroaga et al.* does not otherwise disclose transistor 204 as a decision switch. No other portion of the disclosure of *Iroaga et al.* discloses the function of transistor 204 as a decision switch. Thus, *Iroaga et al.* does not disclose that transistor 204 is a decision switch.

Moreover, *Iroaga et al.* does not disclose "a current path from the first input to the second output." The Examiner has asserted that *Iroaga et al.* discloses that a current path is enabled between the a first input, 205, and the second output, B, however there is no current path between the first input, 205 and the second output, B. Current I_3 which passes through point B does not pass through point 205. *Iroaga et al.* discloses that the gate of transistor 204 is connected through transistor 201 to V_{cc}. Specifically, current I_3 flows through point B, whereas a separate current I_2 flows through transistor 205. There is no current which flows from the second output to transistor 204. Because of this a change in voltage at the first output A cannot enable a current path from the first input 205 to the second output B only when a voltage present at said first output reaches a threshold. Thus, *Iroaga et al.* does not disclose a current path to enable between the first input and the second output.

Thus, it is respectfully submitted that *Iroaga et al.* does not disclose "a decision switch ... enabling a current path from the first input to the second output only when a voltage present at said first output reaches a threshold."

Each of independent claims 1, 13, and 20 contain similar language. Claim 1 recites "a decision switch coupled to the current sink and enabling a current path from the first input to the second output only when a voltage present at said first output reaches a threshold." Claim 13 recites "a decision transistor coupled to the first output and enabling a current path to the second output." Claim 20 recites "steering the control current provided to said first output when said output voltage is below a threshold." Claims 2-12 depend from claim 1. Claims 14-19 depend from claim 13. Claims 21-25 depend from claim 20. It is therefore respectfully submitted that claims 1-25 are not anticipated by *Iroaga et al.*

Based on the above amendments and these remarks, reconsideration of Claims 1-25 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, January 25, 2006.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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